CLAIMS

1. A method for forming a contact comprising:

providing a semiconductor stack including an active layer formed on a first insulator layer, wherein the first insulator layer is formed on a semiconductor substrate;

implanting the semiconductor substrate through the first insulator layer with a first species to form a first doped region within the semiconductor substrate; and

forming a first contact electrically connected to the first doped region.

2. The method of claim 1, further comprising:

etching a portion of the active layer to form a trench opening;

forming a second insulator layer within the trench opening, adjacent the active layer and on the first insulator layer; and

forming a transistor in the active layer.

3. The method of claim 2, wherein implanting further comprises implanting through the second insulator layer and the active layer.

4. The method of claim 2, wherein forming the transistor further comprises:

forming a gate dielectric on the active layer;

forming a gate electrode on the gate dielectric; and

forming a source region in the active layer adjacent a first side of the gate electrode; and

forming a drain region in the active layer adjacent a second side of the gate electrode, wherein the second side is opposite the first side;

and further comprising:

implanting after etching the portion of the active layer and before forming the gate electrode.

5. The method of claim 4, wherein implanting is after forming the second insulator layer.

6. The method of claim 4, wherein the first dopant is p-type.

7. The method of claim 6, wherein the first dopant is boron.

8. The method of claim 7, wherein first dopant is doped using an energy of approximately 100KeV.

9. The method of claim 4, further comprising:

forming an interlayer dielectric layer over the second insulator layer and the active layer;

etching a first opening in the interlayer dielectric layer;

filling the first opening with a metal to form a second contact electrically connected to the active layer; and

wherein forming a first contact further comprises:

etching a second opening through the interlayer dielectric layer, the second insulator layer, and first insulator layer; and filling the second opening with the metal.

10. A method of forming a contact comprising:

providing a semiconductor stack including an active layer formed on a first insulator layer, wherein the first insulator layer is formed on a semiconductor substrate;

forming a gate dielectric over the active layer;

forming a gate electrode over the gate dielectric;

forming source and drain regions in the active layer and adjacent the gate electrode as to form a channel region underneath the gate electrode;

removing a portion of the active layer;

forming a second insulator layer adjacent the active layer and on the first insulator layer;

forming a doped region within the substrate before forming the gate electrode;

forming a first opening in the second insulator layer and the first insulator layer; and

forming a conductive material within the first opening.

11. The method of claim 10, wherein forming a doped region within the substrate comprises implanting a first species through the first insulator.

12. The method of claim 11, wherein forming a doped region within the substrate further comprises implanting the first species through the second insulator layer and the active layer.

13. The method of claim 10, further comprising forming a second opening and filling the second opening to form a contact that is electrically connected to the active layer.

14. The method of claim 10, wherein the doped region is p-type.

15. The method of claim 14, wherein the doped portion is formed by ion implanting boron at an energy of 100KeV.

16. The method of claim 10, wherein the semiconductor stack is silicon-on-insulator.

17. A method of forming a contact comprising:

providing a semiconductor stack including an active layer formed on a first insulator layer, wherein the first insulator layer is formed on a semiconductor substrate;

removing a portion of the active layer;

forming a second insulator layer adjacent the active layer and on the first insulator layer;

forming an opening in the second insulator layer and the first insulator layer;

forming a conductive material within the opening; and

forming a doped region within the substrate under the area of the opening before forming a conductive material within the opening.

18. A semiconductor device comprising:

a semiconductor substrate comprising a doped portion over an undoped portion;

a first insulator layer formed on the semiconductor substrate;

an active layer formed on a first portion the first insulator layer; and

a transistor formed in the active layer and over the doped and undoped portions of the semiconductor substrate.

19. The semiconductor device of claim 18, further comprising:

a second insulator layer formed adjacent the active layer and on a second portion of the first insulator layer;

an interlayer dielectric formed over the transistor and the second insulator;

a first contact formed through the interlayer dielectric, the second insulator layer, the second portion of the first insulator layer and electrically connected to the doped portion of the semiconductor substrate; and

a second contact formed through the interlayer dielectric and electrically connected to the active layer.

20. The semiconductor device of claim 18, wherein the doped portion is doped p-type.

21. The semiconductor device of claim 20, wherein the doped portion is doped using boron and an energy of 100KeV.